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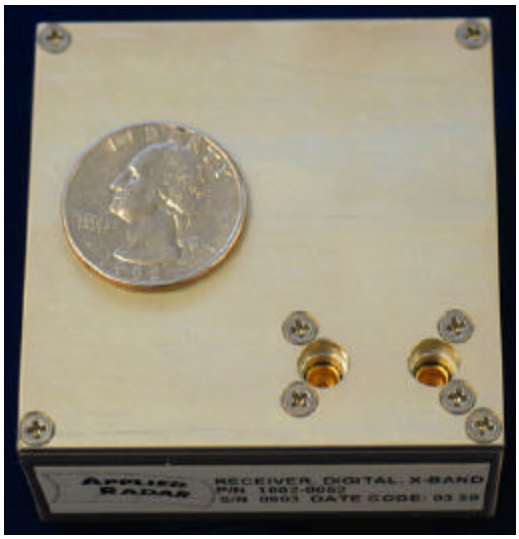
DRX-1000
X-Band Digital Receiver Module

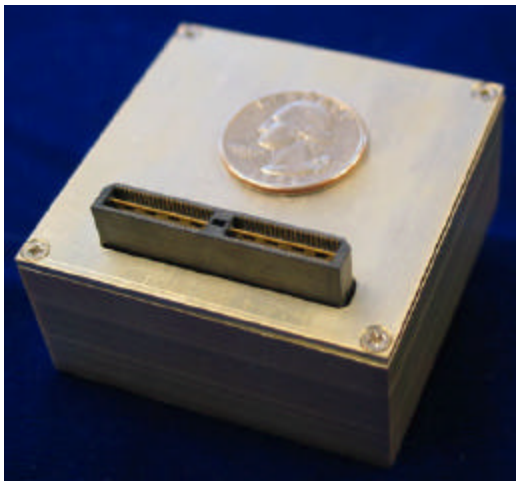
Summary:

The DRX-1000 is a miniature X-band digital receiver module with 15 MHz instantaneous bandwidth and >80 dB dynamic range that takes a X-band (7–12 GHz) RF input and LO signals and outputs real-time digital data. The receiver is composed of a RF and digital sections, which are described separately.

Applications:

Digital radar, software radio, digital beamforming, direction finding (DF), SIGINT. Small size and weight make this receiver ideal for airborne, vehicular, UAV and comm-on-the-move applications. Module is designed to fit behind a 4x4 element subarray of microstrip patch elements.





General Specifications:

Size	2.4”x2.4”x1.2”
Weight	
DC Power	5 Watts
Bandwidth	15 MHz
Freq. Tuning	7 – 12 GHz
Dyn. Range	> 80 dB
SFDR	60 dB
Noise Floor	< –100 dBm
Noise Figure	< 4 dB

Overview:

The DRX-1000 is composed of digital and analog sections, which are described below. The analog section, shown in Figure 1, consists of a single-stage X-band RF downconverter. The X-band RF input signal (7-12 GHz) is amplified, filtered, then downconverted to the IF frequency range 75 MHz +/- 7.5 MHz using an image-reject mixer. The IF output is then amplified and filtered prior to passing to the digital section. The analog section has approximately 30 dB of gain and there is an additional 10 dB of gain in the digital section prior to the A/D.

The LO input frequency controls the tuning of the receiver and is set 75 MHz below the center frequency of the desired RF input. The LO input is also amplified prior to passing to the image-reject mixer so that only a moderate LO input power level (approx. –2 dBm) is required.

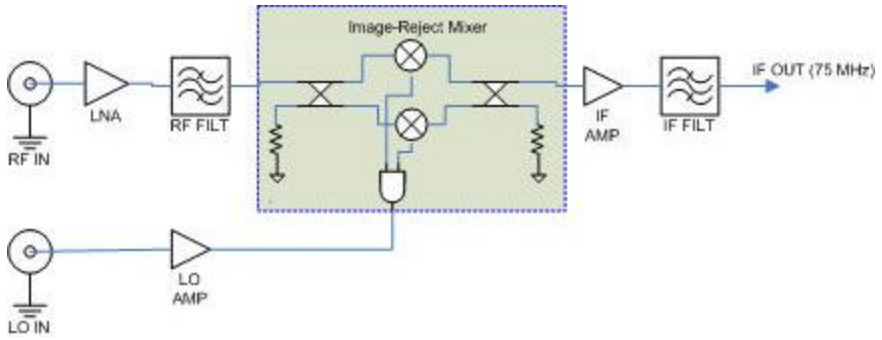


Figure 1: Block diagram of analog section consisting of a single-stage X-band RF downconverter.

Figure 2 shows a block diagram of the digital section. The IF signal output from the analog section is again amplified by about another 10 dB and fed into a 14-bit A/D converter. The data output from the A/D then passes through an FPGA where the data is processed in real-time and sent out the output connector. Typically, the FPGA is used to perform real-time filtering and digital demodulation of the data, resulting in I/Q separation.

The LVPECL clock input is divided into two paths. One path is fed through a digital delay device to the A/D converter. The digital delay is capable of generating up to 1ns of delay in 10ps steps for the purpose of aligning the clock phase of in a multi-channel system (or digital array). A CLK_EN signal is sent to the digital delay device for enabling the clock input to the A/D. The second clock path is fed directly to the FPGA. Phase-aligning of the FPGA input clock may be performed in firmware through the use of a built-in PLL internal to the FPGA.

Additional DATA, ADDR, CONTROL and JTAG signals are provided to the FPGA for controlling various features of the module. These signals are described in more detail below.

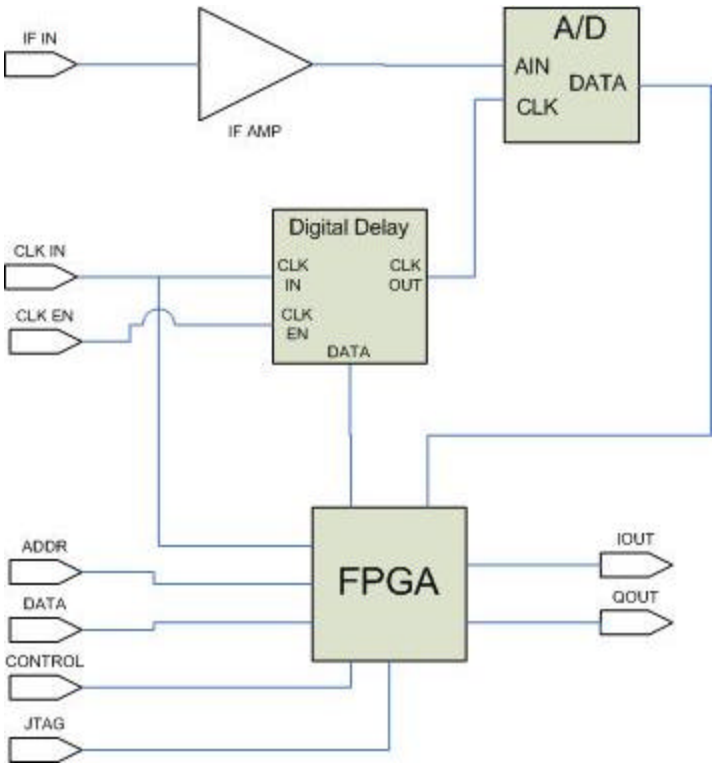


Figure 2: Block diagram of digital section.

Electrical Specifications:

Absolute Maximum Ratings:

DC Power Inputs:	**Min**	**Max**
+1.8V	-0.5V	2.5V
+3.3V	-0.5V	4.6V
+5V_ANALOG		6.0V
+7V_IF		9.0V
+6V_LNA		7.0V
+5V_LO		8.0V
–5V_LO		-6.0V
Digital Inputs:		
ADDR, DATA, CS, RW, etc.	-0.5V	4.6V
Clock Input:		
POS_CLK, NEG_CLK		
RF, LO Inputs:		
RF Input		15 dBm
LO Input		40 dBm

* IMPORTANT: –5V_LO must be applied prior to powering +5V_LO.

Reccomended Operating Parameters:

DC Power Inputs:	**Min**	**Max**
+1.8V	1.71V	1.89V
+3.3V	3.0V	3.6V
+5V_ANALOG	4.85V	5.25V
+7V_IF	6.5V	7.5V
+6V_LNA	5.5V	6.5V
+5V_LO	4.0	6.0
–5V_LO	-5.5	-4.5
Digital Inputs:		
ADDR, DATA, CS, RW, etc.	-0.5V	4.1V
Clock Input:		
POS_CLK, NEG_CLK	0.4Vp-p	
RF, LO Inputs:		
RF Input	-100 dBm	0 dBm
LO Input	-5 dBm	0 dBm

Mechanical Specifications:

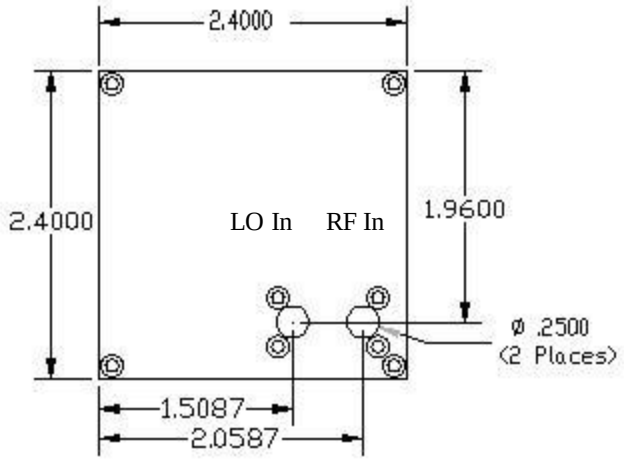


Figure 3: Top view

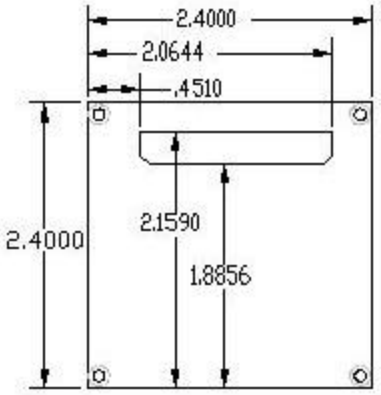


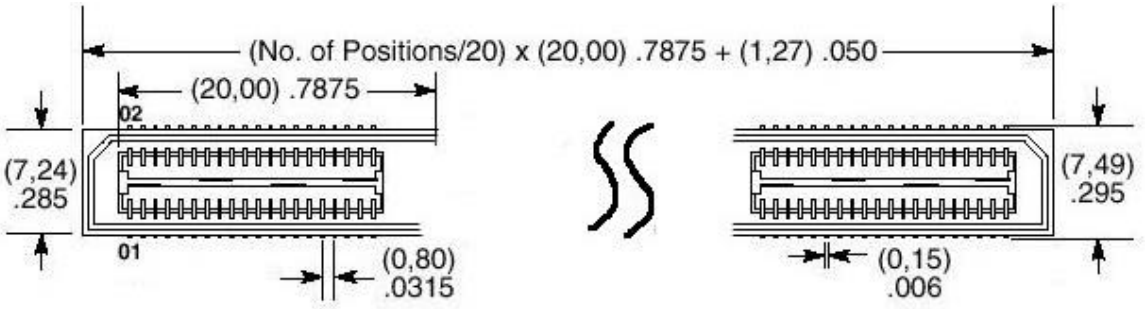
Figure 4: Bottom view

Connector Specifications:

RF+LO Connectors:
GPO Male (www.corning-gilbert.com)

Mating Digital Connector:

SAMTEC QSE-040-L-D-X (www.samtec.com)



(Note pin numbering in figure above)

Figure 5: Digital connector specification.

Digital Pinout:

Pin	Signal Description	Pin	Signal Description
1	IOUT9	2	IOUT8
3	IOUT10	4	IOUT7
5	IOUT11	6	IOUT6
7	IOUT12	8	IOUT5
9	IOUT13	10	IOUT4
11	QOUT0	12	IOUT3
13	QOUT1	14	IOUT2
15	QOUT2	16	IOUT1
17	QOUT3	18	IOUT0
19	QOUT4	20	TCK
21	QOUT5	22	TDO
23	QOUT6	24	TMS
25	QOUT7	26	TDI
27	QOUT8	28	GND
29	QOUT9	30	NEG_CLK
31	QOUT10	32	POS_CLK
33	QOUT11	34	GND
35	QOUT12	36	RESET
37	QOUT13	38	+1.8V
39	DAM_ENABLE	40	+1.8V
41	ADDR0	42	DATA0
43	ADDR1	44	DATA1
45	ADDR2	46	DATA2
47	ADDR3	48	DATA3
49	ADDR4	50	DATA4
51	ADDR5	52	DATA5
53	ADDR6	54	DATA6
55	ADDR7	56	DATA7
57	CS	58	DATA8
59	RW	60	DATA9
61	SYS_RESET#	62	DATA10
63	CONF_DONE	64	DATA11
65	+3.3V	66	DATA12
67	+3.3V	68	DATA13
69	+5V_ANALOG	70	DATA14
71	+5V_ANALOG	72	DATA15
73	GND	74	GND
75	GND	76	+5V_LO
77	+7V_IF	78	–5V_LO
79	+6V_LNA	80	GND

Signal Descriptions:

Power Input Pins:	
GND	Common analog/digital ground. Also tied to mechanical housing.
+3.3V	Digital/Analog 3.3V power input
+1.8V	Digital 1.8V power input
+5V_ANALOG	Analog 5V power input to A/D
+7V_IF	7V supply to IF amplifiers
+6V_LNA	6V supply to LNA
+5V_LO	Pos 5V supply to LO buffer amplifier. Caution: apply Neg 5V prior to powering this signal, then ramp up from DC to +5V. Power down in reverse sequence.
–5V_LO	Neg 5V to LO buffer amplifier. Caution: this signal must be applied prior to powering +5V_LO.
Clock Input:	
POS_CLK,NEG_CLK	LVPECL clock input. Signals are capacitively coupled and terminated at 100 Ohms.
JTAG:	
TCK,TMS,TDI,TDO	JTAG pins for programming FPGA.
CONF_DONE	Indicates device successfully programmed.
Control Signals:	
CS	Chip select – control signal for ADDR/DATA bus.
RW	Read/write – control signal for ADDR/DATA bus.
RESET	Hardware reset.
SYS_RESET#	Software reset.
DAM_ENABLE	Enables clock input to A/D
Control Data Bus:	
ADDR[0..7]	Address bus for controlling digital functions.
DATA[0..7]	Data bus for controlling digital functions.
Output Data Bus:	
IOUT[0..13]	Real-time synchronous data output (inphase)
QOUT[0..13]	Real-time synchronous data output (quadrature)

Typical Performance:

RF Downconverter:

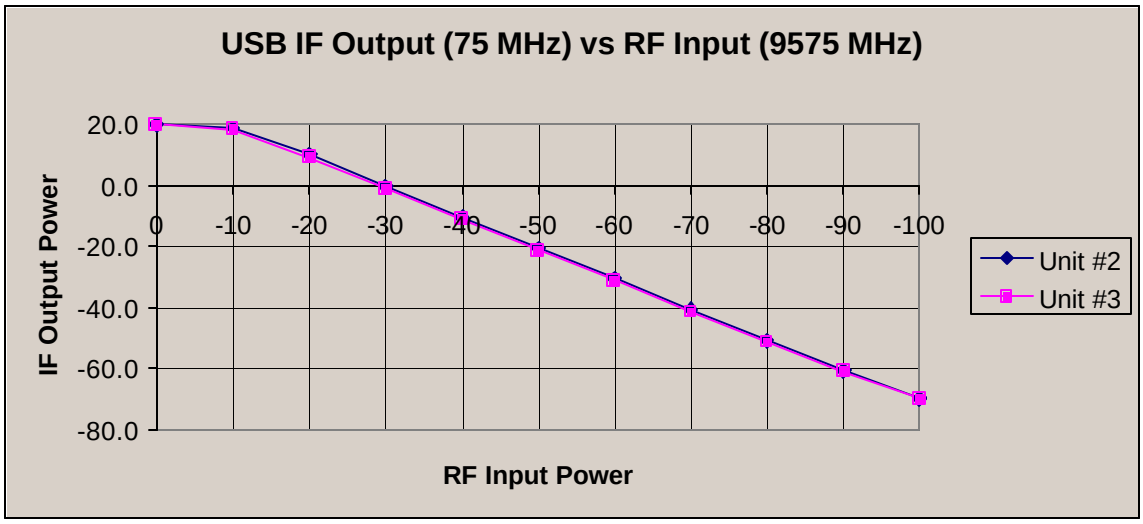


Figure 6: Upper side-band (USB) IF output vs RF input with LO input set at 9500 MHz, -2.0 dBm.

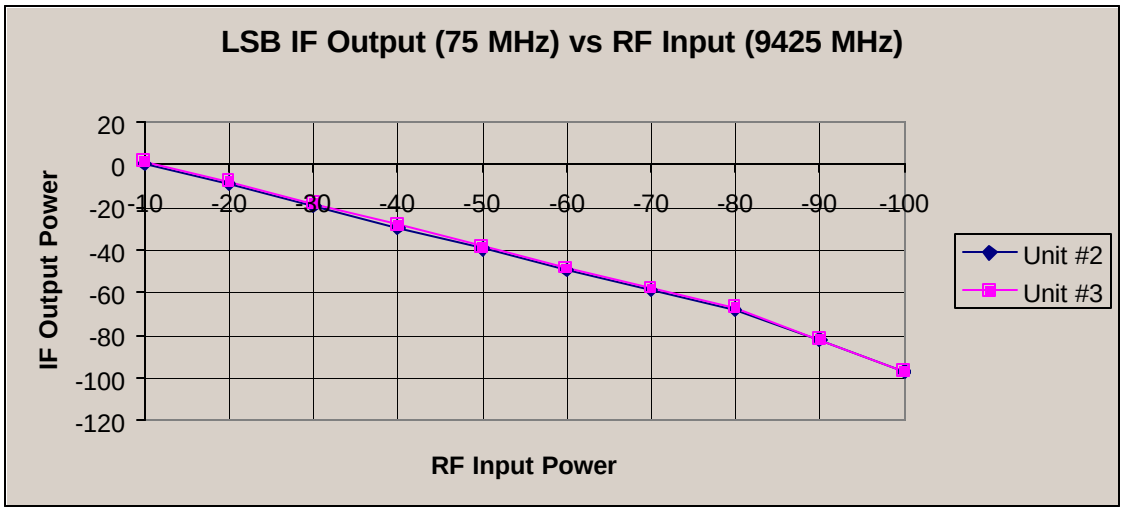


Figure 7: Lower side-band (LSB) IF output vs RF input with LO input set at 9500 MHz, -2.0 dBm.

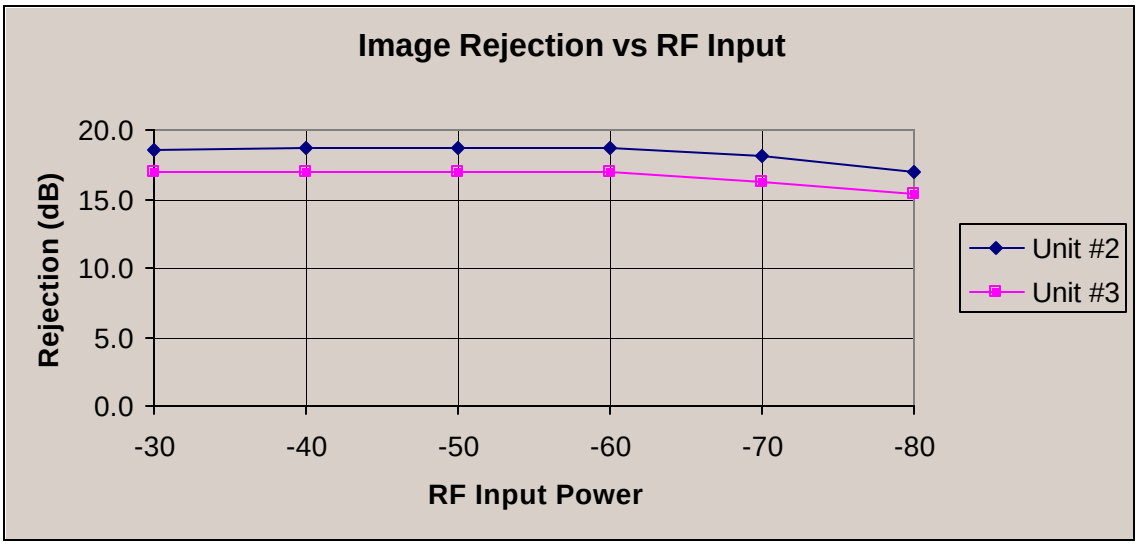


Figure 8: Image-rejection vs RF input power.

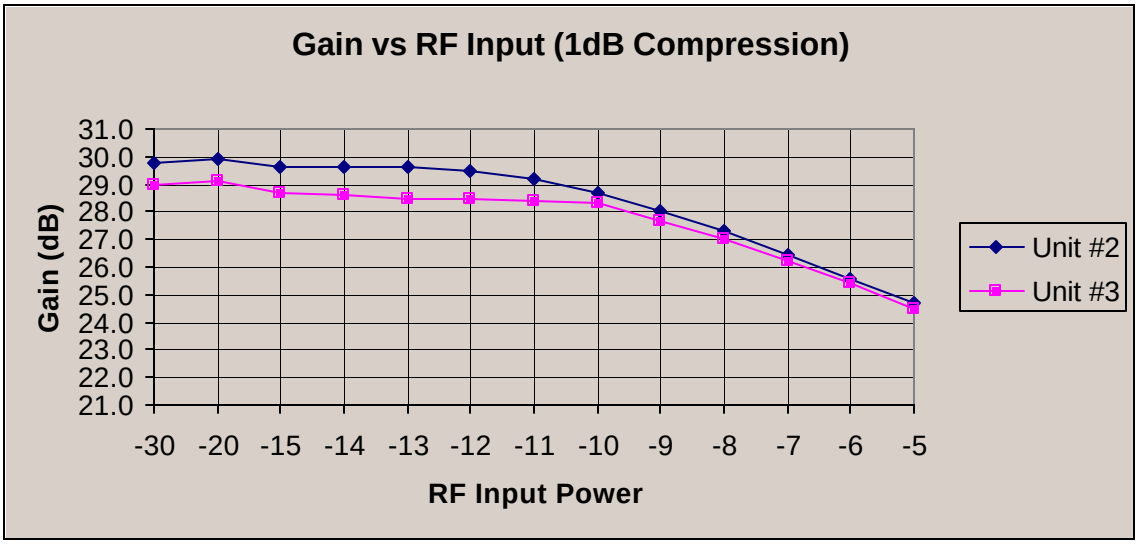


Figure 9: Gain vs RF input power.

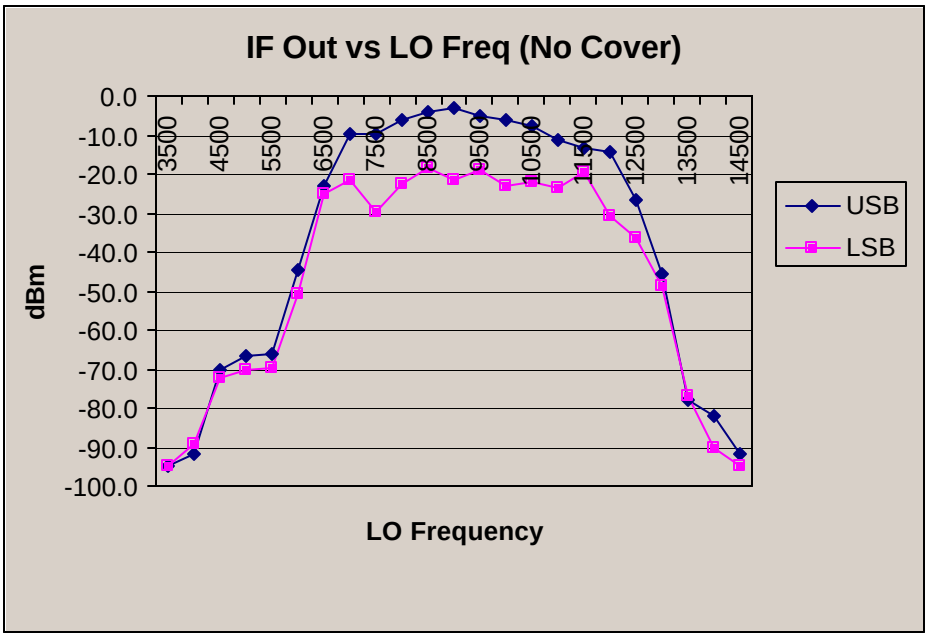


Figure 9: USB/LSB gain vs LO frequency.

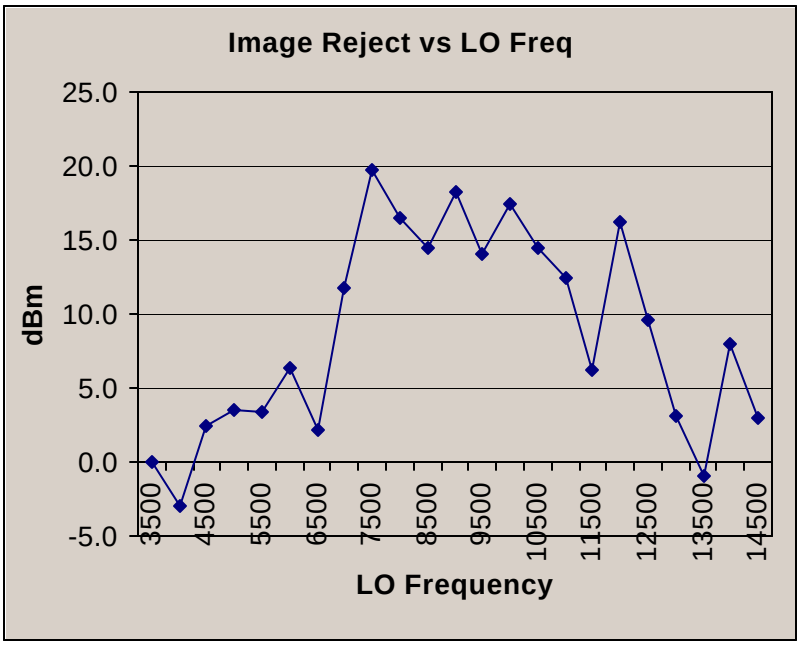


Figure 9: Image-rejection vs LO frequency.

Patent Pending.
Data is preliminary, subject to change.